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A Method for Improving the Settling Time of Phase-locked loop during Acquisition for Communication Systems

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Abstract—*This paper describes a novel method for proportional-integral-derivative controlled phase-locked loop model for communication system for better settling time during acquisition. A proportional-integral-derivative controlled block is inserted in place of a 4th order loop filter of the phase-locked loop. The s-domain transfer function of the system is derived for linear analysis. The settling, phase margin, bandwidth and stability of the system are analyzed through behavioral simulation by using MATLAB platform. It is observed that the proportional-integral-derivative controlled phase-locked loop model reduces the settling time (~ nS) in comparison to phase-locked loop with 4th order loop filter in the loop (~μS).*

Keywords*: Phase Margin, PID controller, PLL, Loop filter, settling time.*

1. INTRODUCTION

The history of the phase-locked loop (PLL) dates back to as early as 1932 by Henri de Bellescize, when British researchers developed an alternative to Edwin Armstrong's super heterodyne receiver, the Homodyne or direct-conversion receiver. In 1970, it became widespread because of the development of integrated circuits (ICs) [1, 13, 14].

The PLL is a very interesting and useful building block available as single integrated circuits in modern communication system design. The PLL is a feedback control system that generates an output signal having a frequency which is synchronized to that of an input reference signal [2, 3, 13, 14]. As shown in **Fig.1**, PLL consists of the four blocks namely: (a) phase detector (PD), (b) loop filter (LF), (c) voltage-controlled oscillator (VCO), and (d) a divide-by-N counter. The PD is a type of multiplier whose output consists of a dc voltage which has the phase information of the input signal. The phase error between the input and output signal is fed to the LF which integrates the signal to smoothen it. The LF output is given to the VCO input. The VCO generates an output signal with a frequency which is proportional to the input voltage. The PLL is considered to be phase locked when

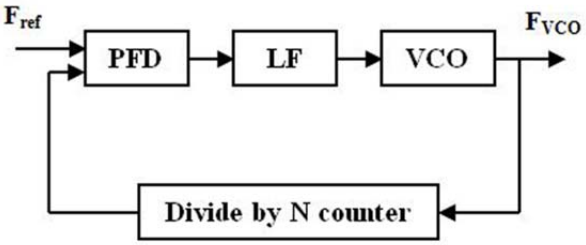

Fig. 1: Block diagram of PLL

the loop phase error is constant and the loop is in stable equilibrium state [2, 14, 15].

PLL are widely employed in radio, computers, telecommunications, satellite communication, airborne navigational systems, frequency modulation and other electronic applications. Frequency synthesis is currently a very important PLL application area. The settling time of PLL plays a significant role in applications which need fast frequency switching as frequency hopping spread spectrum (FHSS) communication system, step frequency radars (SFR) and wireless local area networks (WLANs) [5,6,10,16]. Also, frequency modulated (FM) transceiver application requires carrier frequency and local oscillation frequency with low settling time. Thus, it is necessary to improve the settling time of PLL without effecting the noise performance and power consumption of the system [10]. In this paper we discuss a method to minimize the settling time of PLL system for communication system.

2. REVIEW OF RELATED WORKS

In 2010, K. Kalita, J. Handique, T. Bezboruah and K. Bora described a model for the analysis and software implementation of proportional-integral-derivative (PID) controlled higher order PLL to reduce the settling time up to 76.79%, 54.70% and 43.54% for 2nd, 3rd and 4th order PLL respectively [7].

In 2011, Karuppanan P and Kamala Kanta Mahapatra discussed the compensation process based on PLL synchronization with PID controller based on shunt active power line conditioners under various balanced and unbalanced load conditions [8].

In 2012, Luciane Agnoletti dos Santos, Maurício dos Santos Kaster and Sergio Augusto Oliveira da Silva proposed a model that compares the single-phase PLL algorithm controlled by a conventional PI and a proposed adaptive nonlinear PI to obtain a transient response which is 2.3 times faster than the conventional PI [9].

In 2013, K. Bora and T. Bezboruah proposed a model for modeling and software implementation of highly stable PID controlled 2nd, 3rd and 4th order PLL in the frequency range from 0-0.9GHz to reduce the settling time of 2nd, 3rd and 4th order PLL up to 94%, 49% and 18% respectively with phase margin of 165 degree [10].

In 2014, S. Golestan, M. Monfared, Francisco D. Freijedo, and Josep M. Guerrero developed a systematic and efficient approach to design the control parameters of the synchronous reference frame PLL (SRF-PLL) with pre-filtering stage [11].

In 2015, S. Golestan, Francisco D. Freijedo and Josep M. Guerrero presented a systematic approach to design high-order PLLs control parameters for 1st, 2nd, 3rd and 4thorder LPF respectively and they observed that the reduced-order model provides good accuracy in all cases [12].

3. THE OBJECTIVE AND METHODOLOGY

The main objective of the proposed work is to design and simulate a PID controlled 5th order PLL to decrease the settling time of the PLL system. This is achieved by replacing the loop filter of PLL with a PID controller block during acquisition. Simulation is done on MATLAB platform to study: (i) the stability, (ii) transient behavior, (iii) bandwidth (BW), (iv) phase margin (PM), and (v) settling time of the system.

The methodologies towards implementation of the proposed work are: (i) derivation of s-domain transfer function(TF) for each block of the model, (ii) derivation of generalized TF of the model by integrating individual TF of each block, and (iii) simulation of the model in MATLAB platform to study the various aspects of the system under consideration.

4. THEORETICAL ESTIMATION FOR THE PROPOSED MODEL

The conceptual block diagram of the proposed model is shown in **Fig.2** and 4th order passive LF is shown in **Fig.3.**

4.1. Estimation for PD

The PD block within the PLL compares the phase of the two signals and generates a voltage according to the phase difference between them [3, 4, 14, 15].

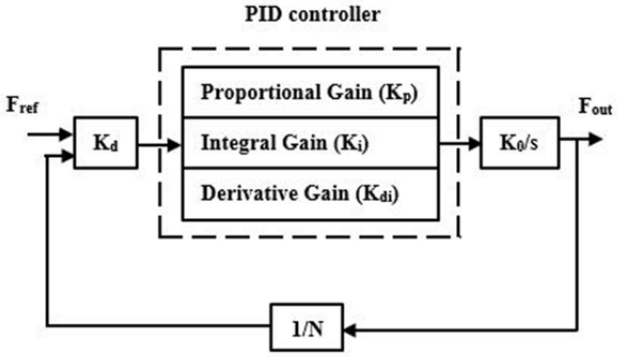

Fig. 2: Functional block diagram of the proposed model

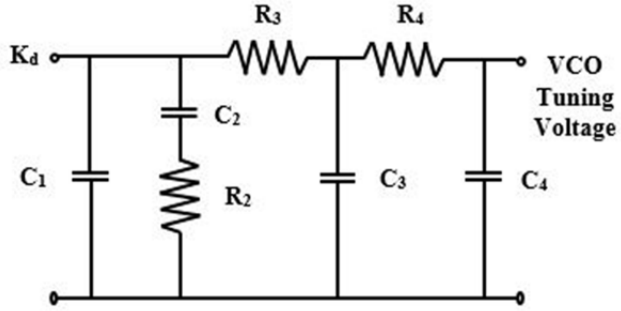

Fig. 3: 4thorder passive LF

The output voltage of PD is calculated as:

$$V_{PD} = K_d \, \phi_e$$

$$K_d = \frac{V_{PD}}{\phi_e} \qquad (1)$$

Where K_d is the PD gain which is measured in volts/radian and φ_e is a phase error between reference signal and VCO output signal.

4.2. Estimation for LF

The LF is a 4th order passive low pass filter (LPF) used to remove any high frequency components of the signals of which the phase is being compared from the VCO output [6]. The transient response of a stable LPF depends on the magnitude of the pole and zero. The number of poles and zeros in LPF verify the type of PLL system [18, 19]. For the proposed model, we have considered a 4th order passive LPF as given in **Fig.3.**

The TF of the 4th order passive LPF can be expressed as [15]:

$$F(s) = \frac{1 + sC_2R_2}{s(A_3s^3 + A_2s^2 + A_1s + A_0)} \qquad (2)$$

Where,

$A_0 = C_1 + C_2 + C_3 + C_4$

$A_1 = C_2R_2(C_1 + C_3 + C_4) + R_3(C_1 + C_2)(C_3 + C_4) + C_4R_4(C_1 + C_2 + C_3)$

$A_2 = C_1C_2R_2R_3(C_3 + C_4) + C_4R_4(C_2C_3R_3 + C_1C_3R_3 + C_1C_2R_2 + C_2C_3R_2)$

$A_3 = C_1C_2C_3C_4R_2R_3R_4$

Hence from the equation (2) the TF for the 4th order LPF can be re-written as:

$$F(s) = \frac{1 + sC_2R_2}{C_1C_2C_3C_4R_2R_3R_4s^4 + \{C_1C_2R_2R_3(C_3 + C_4) + C_4R_4(C_2C_3R_3 + C_1C_3R_3 + C_1C_2R_2 + C_2C_3R_2)\}s^3 + \{C_2R_2(C_1 + C_3 + C_4) + R_3(C_1 + C_2)(C_3 + C_4) + C_4R_4(C_1 + C_2 + C_3)\}s^2 + (C_1 + C_2 + C_3 + C_4)s} \quad (3)$$

4.3. Estimation for PID controller

A PID controller is a widely used control loop feedback system in industrial applications. In PID controller, an error signal is used to generate the proportional, integral and derivative actions of the system [7, 8, 9, 10].

The TF of PID controller can be derived as [20]:

$$T_{PID} = K_p + \frac{K_i}{s} + K_{di}s \quad (4)$$

Where, K_p is proportional gain which will reduce the rise time.

K_i is integral gain which will eliminate the steady-state error.

K_{di} is derivative gain which will reduce the overshoot and settling time.

4.4. Estimation for VCO

The main function of VCO is to generate an oscillating signal proportional to the applied dc control voltage.

The TF of VCO block can be derived as:

$$G_{VCO}(s) = \frac{K_0}{s} \quad (5)$$

Where K_0 is the gain factor of VCO and is given as

$$K_o = \frac{1}{R_oC_o}$$

Where, R_o and C_o are the resistance and capacitance used in VCO design [3, 13, 14, 15].

4.5. Estimation for FD

The frequency divider scales the output frequency by a factor of N. The scaling factor is the relation between the input frequency and the desired output frequency.

The TF of the FD can be derived as:

$$Scale = \frac{f_{in}}{f_{out}}$$

$$F_{FD} = \frac{1}{N} \quad (6)$$

Where, N is the division ratio.

4.6. Estimation TF for the proposed model

The system TF of the proposed model can be derived as:

$$H(s) = \frac{Forward\ \ Gain}{1 + Loop\ \ Gain} \quad (7)$$

4.6.1. TF of PLL with 4th order LPF

The forward gain of the system can be derived as:

$$F_{Gain} = K_dF(s)\frac{K_o}{s} \quad (8)$$

The loop gain is calculated from the product of the individual TF of each block of PLL and can be expressed as:

$$L_{Gain} = \frac{K_dK_oF(s)}{Ns} \quad (9)$$

Combining equations (3), (7), (8) and (9), the TF of PLL with 4th order passive LPF can be derived as:

$$H_{4th}(s) = \frac{K_dK_o(1 + sC_2R_2)}{C_1C_2C_3C_4R_2R_3R_4s^5 + \{C_1C_2R_2R_3(C_3 + C_4) + C_4R_4(C_2C_3R_3 + C_1C_3R_3 + C_1C_2R_2 + C_2C_3R_2)\}s^4 + \{C_2R_2(C_1 + C_3 + C_4) + R_3(C_1 + C_2)(C_3 + C_4) + C_4R_4(C_1 + C_2 + C_3\}s^3 + (C_1 + C_2 + C_3 + C_4)s^2 + KC_2R_2S + K} \quad (10)$$

Where, $K = \frac{K_dK_o}{N}$ = Loop Gain constant [16] (11)

4.6.2. TF of the PLL with PID controller

For the TF of the proposed PID controlled PLL model can be derived by using equations (4), (7), (8), (9) and (11) and can be expressed as:

$$H_{PID}(s) = \frac{K_dK_o(K_{di}s^2 + K_ps + K_i)}{s^2(1 + K_{di}K) + K_pKs + K_iK} \quad (12)$$

5. THE SIMULATIONS

The behavioral simulations have been carried out on the TF functions of the model given in equation (10) and (12), by considering both PID controlled PLL and PLL with 4th order

LF. The s – domain TFs are simulated using MATLAB to study different characteristics of the model. The specification of the design parameters for different test cases of the PID controller PLL model and PLL with 4th order LF are given in **Table 1** and **Table 2** respectively. **Table 3** shows the constant parameters of the model for both cases. We have considered different parameters, namely: (a) PFD gain: K_d, (b) VCO Sensitivity: K_o, (c) fractional counter value: N, (d) 4th order LF components: R_2, R_3, R_4, C_1, C_2, C_3, C_4, and (e) PID controller gain components: K_P, K_i, K_{di} to analyze the behavior of the model.

Table 1: Different parameters of 4th order LF PLL

SL No	C_1 (pF)	C_2 (nF)	C_3 (pF)	C_4 (pF)	R_2 (Ω)	R_3 (Ω)	R_4 (Ω)
1	74	8	0.01	9	10	60	60
2	50	8	0.1	9	8	60	60
3	174	12	0.01	9	2	60	60
4	174	12	0.5	16	5	60	60
5	140	16	1.2	10	7	70	70
6	223	5	0.8	6	7	70	70
7	453	10	0.11	3	9	70	70
8	60	2.8	1.23	1.7	9.8	100	100
9	320	33	0.4	25	5	70	70
10	320	41	2.3	14	4	70	70
11	54	21	2.3	29	4	90	90
12	100	12	0.62	5	8	90	90
13	410	8.2	0.06	.7	5.5	90	90
14	23	6	0.34	22	9	90	90
15	23	267	4.2	2	12	100	100
16	77	22	0.7	8	7	100	100
17	150	15	0.4	2	11	120	120
18	87	4	0.5	1.2	12	120	120
19	34	1080	0.01	5	10.8	120	120
20	105	4	0.5	1.2	12	120	120
21	76	980	0.046	8.5	8	170	170
22	31	700	0.1	2.6	12	170	170
23	53	864	0.1	1.3	10	170	170
24	57	700	0.1	3	14.6	170	170
25	43	463	0.6	1	17	170	170
26	26	782	0.2	2.5	13	230	230
27	28	800	0.7	3.3	8	230	230
28	32	411	0.53	0.2	23.9	250	250
29	20	275	0.02	0.07	35	250	250
30	19	209	0.19	0.5	26	250	250

Table 2: Different parameters of PID controlled PLL

SL No	K_p	K_i	K_{di}
1	101	377e9	30e-11
2	108	900e9	10e-12
3	97	250e9	66e-12
4	99	347e9	3.8e-11
5	100	500e9	500e-11
6	140	600e9	19.8e11
7	149	700e9	35e-11
8	131	610e9	200e-11
9	105	270e9	58e-11
10	125	888e9	56e-12
11	97	763e9	7e-12
12	120	555e9	7e-11
13	100	450e9	24e-11
14	98	233e9	30e-11
15	90	245e9	15e-11
16	150	500e9	78e-12
17	150	10009	22e-11
18	112	259e9	20e-12
19	100	780e9	546e-11
20	109	400e9	63e-11
21	108	403e9	3e-12
22	100	900e9	25.5e10
23	120	376e9	1.6e-12
24	110	293e9	6.4e-11
25	109	10009	100e-10
26	111	992e9	70e-10
27	130	850e9	60e-10
28	108	390e9	44e-12
29	108	303e9	14e-11
30	98	307e9	40e-11

Table 3: Constant parameters of the model

Kd (V/rad)	K0 (MHZ/V)	N
2	20	5

5.1 Simulation for settling time

Settling time is very important parameter for data acquisition systems. In data acquisition system, it is the primary factor which defines the data rate for a process variable to settle within a certain percentage (commonly 5%) of given error level [14, 19]. The study of the step response gives the information about stability and ability to reach steady state of the system. The settling time depends on the LF components, K_d, k_0 and N. In control system settling time depends on plant gain and values of controller parameters. Higher values of K_i parameter provide shorter settling time for the cost of higher controller output time of PLL with PID controller. The step response is commonly used to determine the settling time of the system. Some step responses of simulation for PLL with 4th order LF and with PID controller are shown in **Fig. 4(a)** and **Fig. 4(b)** respectively.

5.2 Simulation for PM and BW of the system

Bode diagrams are a powerful tool for direct assessment of the loop's PM and BW [14]. PLL may be stable or unstable depending on PM value. The PLL system is stable for positive value of PM and unstable for negative value of PM. Small PM always leads to extended transient response in time domain [13, 14]. BW is the modulation frequency at which the PLL begins to lose lock with the changing reference (-3dB). A narrow BW is capable of rejecting large amount of noise [14, 15]. The simulation result of Bode responses for PM of the model for few test cases is shown in **Fig. 5(a)** and **Fig. 5(b).**

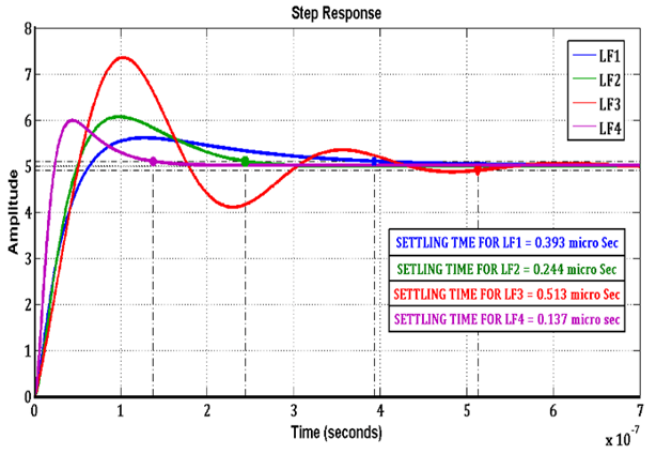

Fig. 4 (a). Step responses of the simulated 4th order LF PLL model

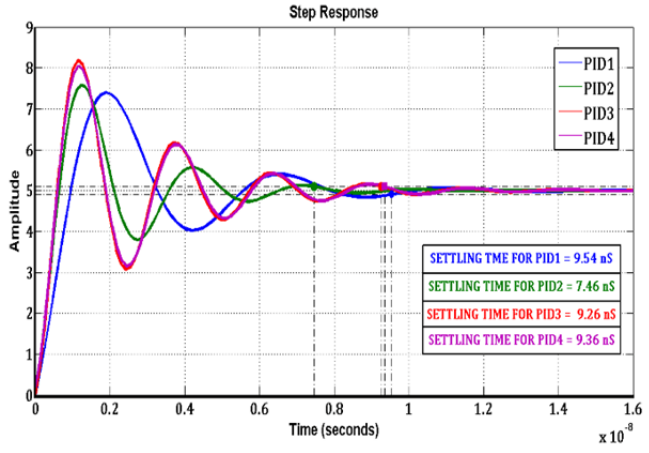

Fig. 4 (b). Step responses of the simulated PID controlled PLL model

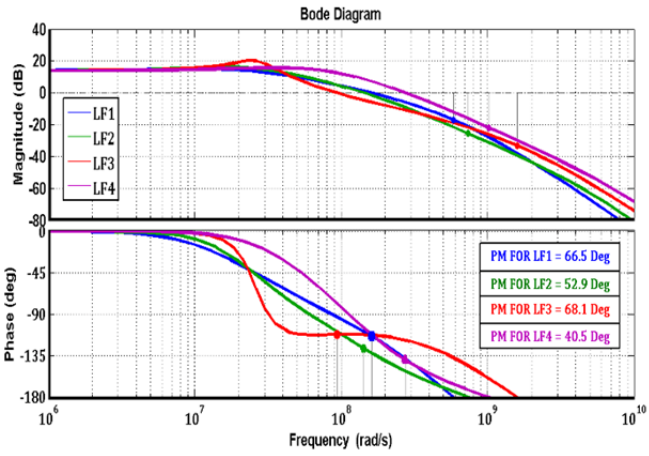

Fig. 5 (a). Bode responses of the simulated 4th order LF PLL model

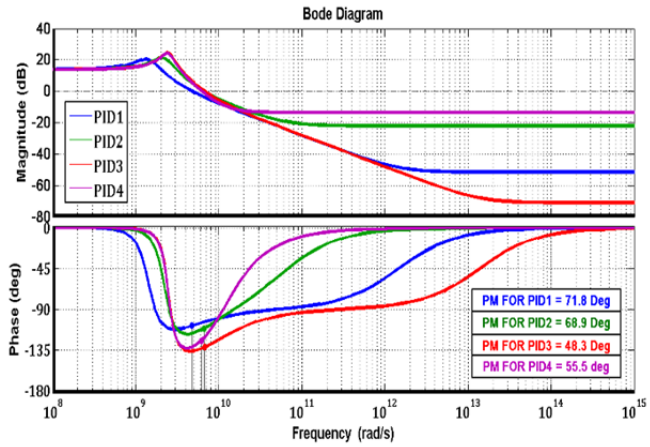

Fig. 5 (b). Bode responses of the simulated PID controlled PLL model

6. RESULTS AND DISCUSSION

The results obtained from analysis of the simulated responses for different test cases of PLL with 4th order LF and PID controlled PLL model are given in **Table 4**. It is observed that the PID controlled PLL model gives better settling time (5.79 nS – 9.94 nS) as compared to the PLL model with 4th order filter in the loop (0.011 µS – 0.513 µS). The stability of a system is related to the PM value of the system. The standard limit of stability for PM value is considered to be in the range 20 – 80 degree [13, 15]. From the simulated responses it is observed that PID controller PLL model gives better PM (48.3º - 76.7º) as compared to that of the PLL model with 4th order LF (40.5º – 77.5º) in the loop. So PID controller PLL model provides better stability.

Table 4: Simulated results for 4th order LF and PID controller PLL model

SL No	PLL Parameters					
	PM (Degree)		Settling Time		Bandwidth (GHz)	
	LF	PID	LF (µS)	PID (nS)	LF	PID
1	56.9	65.3	0.176	9.46	0.0170	0.4442
2	69.6	49.3	0.172	8.50	0.0138	0.6753
3	68.1	71.8	0.513	9.54	0.0068	0.3676
4	62.8	65.8	0.187	9.78	0.0097	0.4279
5	58.8	65.4	0.249	9.94	0.0118	0.4853
6	56.3	69.2	0.117	6.23	0.0142	0.5652
7	40.7	68.8	0.196	5.79	0.0166	0.6088
8	70.9	68.9	0.090	7.46	0.0189	0.5569
9	45.8	74.4	0.356	9.11	0.0090	0.3818
10	66.5	55.7	0.393	7.40	0.0067	0.6747
11	52.9	48.3	0.244	9.26	0.0080	0.6212
12	65.6	64.0	0.216	7.83	0.0131	0.5394
13	67.9	61.0	0.153	8.82	0.0107	0.4825
14	40.5	74.1	0.137	9.78	0.0181	0.3558
15	68.5	69.3	0.035	9.75	0.0172	0.3615
16	64.2	75.4	0.293	6.55	0.0112	0.5249

17	51.3	61.2	0.224	5.91	0.0182	0.7196
18	61.6	76.7	0.121	8.77	0.0207	0.3796
19	63.0	55.5	0.039	9.36	0.0159	0.5979
20	57.8	67.9	0.121	9.09	0.0210	0.4577
21	48.5	66.3	0.072	9.03	0.0130	0.4618
22	65.7	49.1	0.036	9.69	0.0174	0.6576
23	77.5	72.1	0.045	7.76	0.0138	0.4516
24	43.3	73.7	0.026	8.71	0.0240	0.3999
25	55.6	58.5	0.024	9.45	0.0259	0.6508
26	57.9	56.4	0.032	9.28	0.0197	0.6650
27	67.5	66.7	0.052	7.66	0.0116	0.6272
28	52.0	67.0	0.016	9.10	0.0376	0.4546
29	55.5	70.6	0.011	8.33	0.0554	0.4220
30	54.6	68.6	0.015	8.75	0.0399	0.4027

7. CONCLUSION

From the present study of our proposed model by considering PID controlled and 4th order LF in the loop, we can conclude that PID controlled PLL system is highly stable with faster settling time (~nS) and better PM value as compared to that of the 4th orders LF in the loop. So, the model may be suitable for high frequency FM transceiver and industrial applications.

8. ACKNOWLEDGEMENT

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